Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently Amended) Security system for checking authorization, the system including a number of secure devices, each of said secure devices comprising a chip with logic circuitry, having a function in providing authorization to the security system by performing one or more algorithms and logic to provide the authorization, characterized in that in at least a part of said secure devices, the same algorithms and logic are implemented in different chips with a circuitry layout that is unique to each different chip, wherein at least said logic circuitry of the chips of said part of the secure devices is implemented in Field Programmable Gate Array (FPGA) technology, wherein the layout is programmed in the FPGA circuitry in at least one of a volatile and a non-volatile manner. ~~chip of a secure device is provided with a unique chip circuitry layout implementing the same algorithms and logic.~~

2. (Cancelled)

3. (Currently Amended) Security system according to claim ~~2~~1, wherein the logic circuitry of each secure device chip is provided in a secure cell of the chip.

4. (Original) Security system according to claim 1, wherein the complete secure device ship is implemented in FPGA technology, wherein the layout is programmed in the chip in at least one of a volatile and a non-volatile manner.

5. (Currently Amended) Security system according to claim ~~2~~1, 3 or 4, wherein the logic circuitry or the entire chip is made as a volatile programmable FPGA, wherein the FPGA program is stored in a battery powered RAM

6. (Currently Amended) A set of secure devices for a security system according to claim 1, wherein each of said secure devices comprises a chip with logic circuitry having

a function in providing authorization to the holder of a secure device by performing one or more algorithms and logic to provide the authorization, wherein in at least a part of said secure devices, the same algorithms and logic are implemented in different chips with a circuitry layout that is unique to each different chip, wherein at least said logic circuitry of the chips of said part of the secure devices is implemented in Field Programmable Gate Array (FPGA) technology, wherein the layout is programmed in the FPGA circuitry in at least one of a volatile and a non-volatile manner. ~~chip of each secure device is provided with a unique chip layout implementing the same algorithms and logic.~~

7. (Cancelled)

8. (Currently Amended) Method for manufacturing a number of secure ~~device~~ devices for a security system according to claim 1, wherein secure devices with a chip are used, said chips having logic circuitry having a function in providing authorization to the security system by performing one or more algorithms and logic to provide the authorization, wherein in at least a part of said secure devices, the same algorithms and logic are implemented in different chips with a circuitry layout that is unique to each different chip, wherein at least said logic circuitry of the chips of said part of the secure devices is implemented in Field Programmable Gate Array (FPGA) technology, wherein the layout is programmed in the FPGA circuitry in at least one of a volatile and a non-volatile manner. ~~the chip of a secure device is provided with a unique chip circuitry layout implementing the same algorithms and logic.~~

9. (Currently Amended) Method according to claim 8, ~~wherein chips with logic circuitry in FPGA technology are used,~~ said method comprising the steps of programming a unique information in the logic circuitry by means of a synthesis tool and a layout tool, wherein for each secure device of said part of secure devices, a variation factor is introduced in at least one of the synthesis tool and the layout tool, thereby providing a unique circuit layout.

10. (Original) Method according to claim 9, wherein the synthesis tool is provided with input information compiled from a high level language code, wherein a variation factor is introduced in at least one of the compilation step of the high level language code, the synthesis tool and the layout tool.